27.4 An 80nm 4Gb/s/pin 32b 512Mb GDDR4 Graphics DRAM with Low-Power and Low-Noise Data-Bus Inversion

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The 3D graphics application demands a low-cost and high-bandwidth DRAM, which is implemented by extending the number of single-ended I/Os. However, the DRAM suffers from the bottlenecks of parallel single-ended signaling, such as simultaneous switching noise (SSN) [1], crosstalk, reference-voltage (V_{ref}) noise, and deterministic jitter due to inter-symbol interference (ISI) and duty-cylce distortion. To increase the speed of parallel single-ended signaling, we implement an 80nm 32b 512Mb GDDR4 DRAM with a low-power and low-noise data bus inversion (DBI) scheme [2] with an analog majority voter that is insensitive to mismatch, a dual duty-cycle corrector (DCC) to average DCC error, and a tunable off-chip driver (OCD) and on-die termination (ODT) [2] to obtain an effect similar to V_{ref} calibration with minimal overhead.

DBI DC [3], shown in Fig. 27.4.1, restricts the number of zeros in parallel data to a maximum of four. DBI AC [4], also shown in Fig. 27.4.1, restricts the number of transitions between previous and present data to a maximum of 4. DBI DC reduces the average and peak current draw because V_{DDQ} termination I/O does not require DC current flow when driving high. Both $L \cdot \frac{di}{dt}$ noise and crosstalk are also reduced since the number of concurrent data transitions with the same direction is no more than four. In an environment where switching noise is dominant, such as a channel without a termination resistor, DBI AC is more effective than DBI DC. DBI also reduces V_{ref} noise caused by SSN and crosstalk. Figure 27.4.1 shows the proposed dual modes encoding circuit, which consists of eight DBI blocks with 64b input data to accommodate the 8b burst length of GDDR4. Both DBI DC and AC modes are combined in a single DBI circuit and mode selection is determined by the termination condition. While DBI DC mode is simple and operates at high speed, the maximum operation speed of DBI AC mode is limited by the delay of the majority voter, latch, and inversion circuit because of the sequential comparison between the present DBI input and previous DBI output [4]. To solve this problem, the DBI encoding circuit converts the sequential comparison to a parallel comparison that compares Din[n] with Din[n-1] rather than Dout[n-1]. Furthermore, the DBI_flag[n] is determined by the majority voter output and the previous DBI_flag[n-1]. When DBI_flag[n-1] is 0, DBI_flag[n] is the majority voter output because Dout[n-1] is the same as Din[n-1]. But, when DBI_flag[n-1] is 1, DBI_flag[n] is the inversion of majority voter output because Dout[n-1] is the inversion of Din[n-1].

The majority voter is implemented as an analog amplifier with segmented and equal-sized offset input transistors, which avoids the high area overhead and computational delay of a digital implementation [3]. However, when the number of 1s is four, errors occur due to the mismatch of transistors, since the size ratio of the input transistors turned on between two branches is 4:5. Moreover, the maximum data rate is limited by the increasing delay time of the majority voter due to its low gain. Figure 27.4.2 shows the proposed analog majority voter insensitive to the mismatch, where PMOS loads as well as NMOS inputs are divided into 16 segments and the MOSFET size of two branches are different. The output current difference of the proposed majority voter has higher amplification than that of the conventional majority voter because of the PMOS loads with unequal size. When the number of 1s is four, the effective size ratio between two branches is increased from 1:1.25 to 1:1.65. So the errors due to the mismatch and the delay time of DBI reduce significantly.

GDDR4 DRAM has a source-synchronous clocking scheme, which has the benefit of jitter tolerance, however, when there is duty-cycle distortion in clock, timing margin is reduced by twice the amount of the duty-cycle distortion. The duty-cycle distortion is reduced using a duty-cycle corrector (DCC), however, the correction is limited by the offset of the duty cycle detector (DCD) and the jitter caused by control voltage fluctuation, which is severe at low frequencies [5]. A differential DDR clocking scheme, shown in Fig. 27.4.3(a), is immune to DCD offset. Even though there is the offset of DCD, the offset is not seen. This is accomplished by interpolating differential clock signals whose duty cycle is corrected independently. When the duty cycles of CLK and CLKb are a and b, respectively, the output duty of the phase interpolator is reduced to the average value of a and $1–b$. The low-frequency jitter caused by control voltage fluctuation in the duty-cycle detector is also reduced by the interpolation of CLK rising shape and CLKb falling shape whose jitter is opposite. Figure 27.4.3(b) shows the duty cycle of the output clock according to the offsets of two DCDs. Usually two DCD offsets have the same polarities because two DCDs are very close, and the duty distortion of output clock is reduced.

R_{on} tuning is incorporated in GDDR4 DRAM to have higher noise margin at receiver. R_{on} tuning is implemented by adding a user-supplied R_{on} offset value to the auto-calibrated R_{on} value [6] shown in Fig. 27.4.4(a). R_{on} tuning of the OCD and ODT, is similar to V_{ref} calibration. If V_{ref} is away from the optimum level, through R_{on} tuning, the crossing point of a signal is tuned to V_{ref} level. Furthermore, R_{on} tuning cancels out the offset value of OCD and ODT due to PVT variation. Figure 27.4.4(b) shows the optimum R_{on} value with the maximum aperture window. This simulation result shows that R_{on} tuning for V_{ref} optimization is more effective than impedance matching between channel and termination in a short channel. Direct V_{ref} calibration requires extra area overhead, but R_{on} tuning is easily merged to the R_{on} auto-calibration circuit.

In addition, to reduce the ISI caused by a large C_{in}, the OCD and ODT are shared as in [6] and the ratio between resistance and active transistor in OCD and ODT is optimized to have small amount of active transistor without hurting the channel margin. C_{in} is reduced to 1.5pF. Multi-cycle preamble [2] is helpful to make a correct data sampling strobe by generating the preamble of the strobe several cycles ahead of DQ signals to reduce ISI of the strobe signal. The skew caused by a clock tree is predicted and controlled by chip-level parasitic extraction of the clock tree. Less than 60ps per-pin skew is achieved.

Figure 27.4.5 shows the measured eye patterns of read operation at the data rate of 4Gb/s with and without DBI DC encoding, of which data patterns are same. DBI DC reduces peak-to-peak jitter from 65.5ps to 44.5ps and voltage fluctuation from 183mV to 115mV. Voltage fluctuation of the data signal decreases both voltage and timing margins severely, since the data signal is compared to the external reference voltage made from an off-chip supply voltage in single-ended signaling. While the two crossing points of signal in Fig. 27.4.5(a) have different voltage levels, the two crossing points of signal in Fig. 27.4.5(b) have similar voltage levels. The measured duty distortion is around 10ps. Figure 27.4.6 shows the shmoo plot at room temperature. The maximum data rate with a read latency of 21 is 4Gb/s at 2V. Figure 27.4.7 shows the micrograph of the fabricated 16M×32b GDDR4 SDRAM in an 80nm CMOS process.

References:

[1] J.-Y. Sim and W. Namgoong, "Multilevel Differential Encoding With Precentering for High-Speed Parallel Link Transceiver," *IEEE J. of Solid-State Circuits*, vol. 40, no. 8, pp. 1688-1694, Aug., 2005.
[2] Graphics Double Data Rate 4 (GDDR4) SGRAM Specification, JEDEC.
[3] K. Nakamura and M.A. Horowitz, "A 50% Noise Reduction Interface Using Low-Weight Coding," *Symp. VLSI Circuits,* pp. 144-145, Jun., 1996.
[4] M.R. Stan and W.P. Burleson, "Bus-Invert Coding for Low-Power I/O," *IEEE Transaction on VLSI Systems*, vol. 3, no. 1, pp. 49-58, Mar., 1995.
[5] B.-G. Kim, K.-I. Oh, L.-S. Kim, and D.-W. Lee, "A 500MHz DLL with Second Order Duty Cycle Corrector for Low Jitter," *IEEE CICC*, pp. 325-328, Sep., 2005.
[6] C. Park, H.-J. Chung, Y.-S. Lee, et al, "A 512-Mb DDR3 SDRAM Prototype with C_{IO} Minimization and Self-Calibration Techniques," *IEEE J. of Solid-State Circuits*, vol. 41, no. 4, pp. 831-838, Apr., 2006.

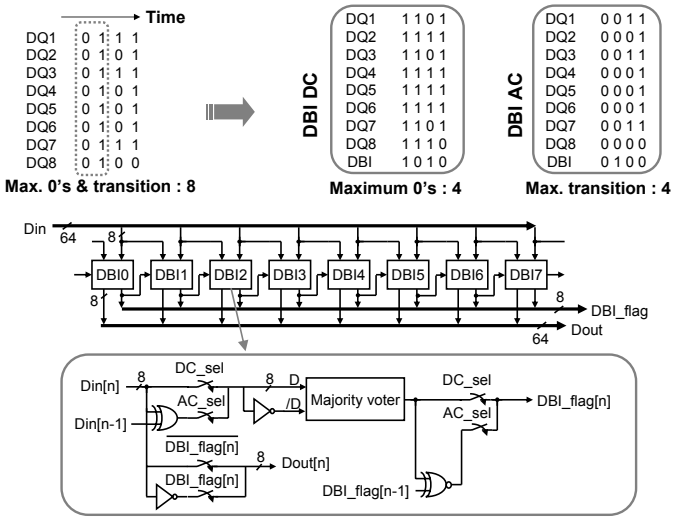


Figure 27.4.1: Encoding algorithm and circuit of DC and AC data-bus inversion.

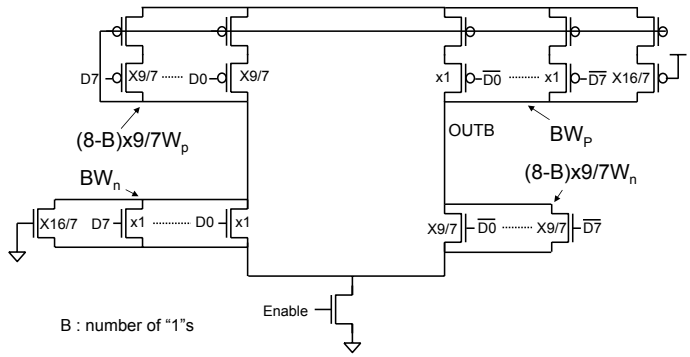
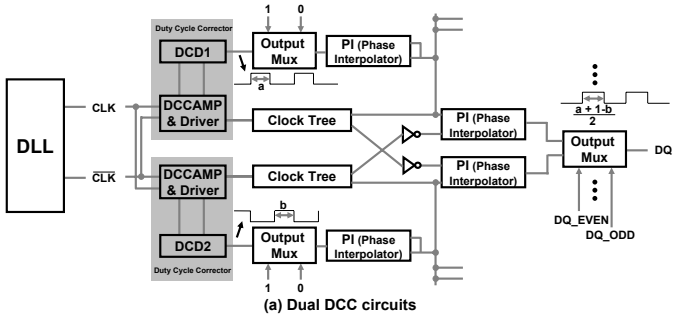


Figure 27.4.2: Proposed analog majority voter.

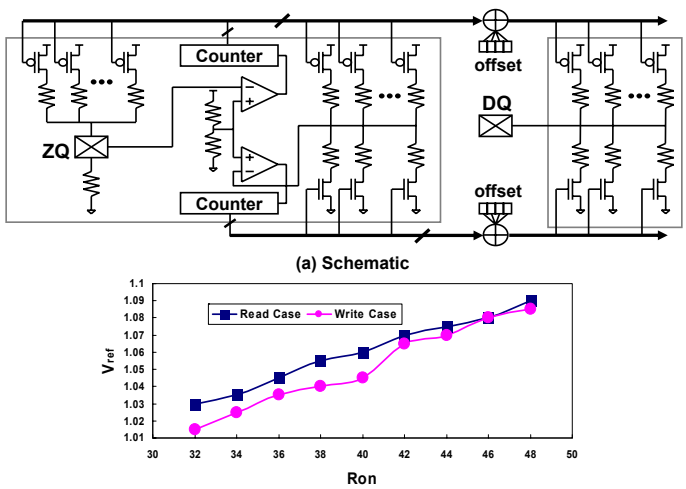


(a) Dual DCC circuits

DCD1 offset	DCD2 offset	Duty a	Duty b	(a+1-b)/2
5%	5%	45%	45%	50%
5%	0%	45%	50%	48.5%
5%	-5%	45%	55%	45%

(b) Duty cycle of output clock vs. offset of DCD

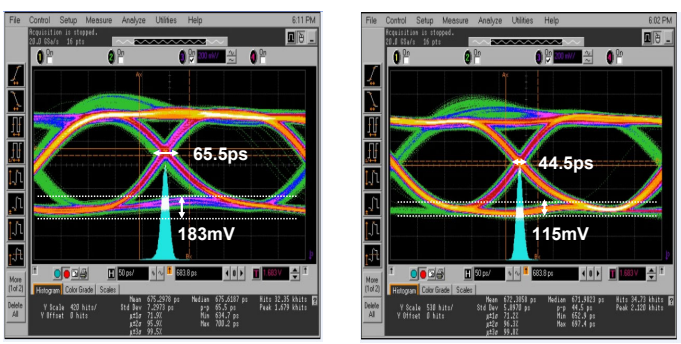
Figure 27.4.3: Differential DDR clocking scheme and its duty cycle correction scheme.



(a) Schematic

(b) V_{ref} vs. Ron with Max. aperture window

Figure 27.4.4: R_{on} tuning -OCD and ODT offset control.



(a) Without DBI

(b) With DBI DC

Figure 27.4.5: Measurement results of eye pattern at the data rate of 4Gb/s.

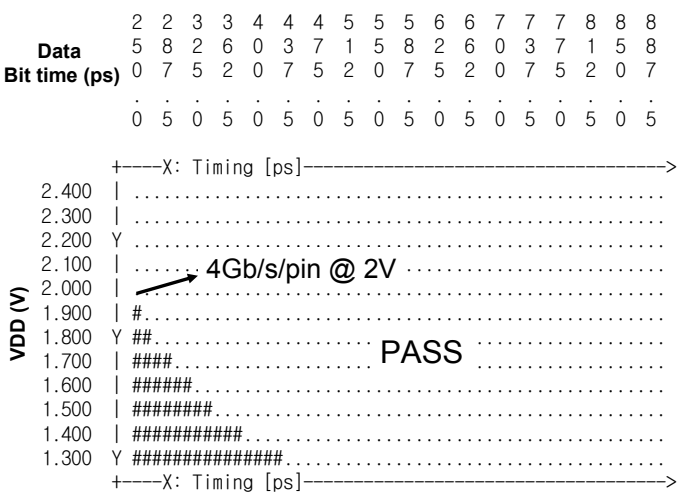


Figure 27.4.6: Shmoo plot.

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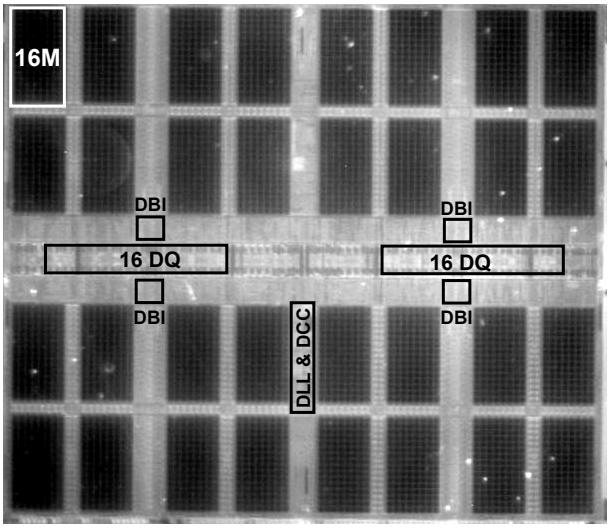

Figure 27.4.7: Chip micrograph.

